

IN THE CLAIM

1 1. (Previously Amended Once, Currently Amended) A method for retiring a first
2 instruction[s] processed through various processing stages, comprising the steps
3 of:
4 processing a second instruction different from the first instruction;
5 processing an the first instruction ~~capable of early retirement~~ until the first
6 instruction meets the criteria for early retirement;
7 indicating that the first instruction has met the early-retirement criteria;
8 processing the first instruction to a desirable stage, and at which, based on
9 an the indication that the first instruction has met the early-
10 retirement criteria, terminating the first instruction is terminated out
11 of order of a program running the first instruction; and
12 updating a state of a system processing the first instruction to reflect that
13 the first instruction has been terminated;
14 wherein the early-retirement criteria is met when processing the second
15 instruction causes the instruction is processed to a point that
16 continued processing of the first instruction does not change the an
17 architectural state of the system processing the first instruction,
18 and, at the time of termination, the first instruction has completed
19 its function without completing its full pipeline.

1 2. (Currently Canceled)

1 3. (Original) The method of claim 1 wherein the step of indicating comprises the step of
2 generating a signal associated with the instruction.

- 1 4. (Currently Amended) The method of claim 3 further comprises the steps of:
2 sending the signal to an early-retirement unit; and
3 the early-retirement unit arranging for the first instruction to be terminated.
- 1 5. (Original) The method of claim 1 wherein the various processing stages include one or
2 more of the following stages: fetching, issuing, sorting, executing, queuing, and
3 retiring.
- 1 6. (Currently Amended) The method of claim 1 wherein [the] an instruction capable of
2 early retirement includes an identification tag for identifying whether the
3 instruction is capable of early retirement.
- 1 7. (Currently Canceled)
- 1 8. (Previously Canceled)
- 1 9. (Currently Canceled)
- 1 10. (Previously Amended Once, Currently Amended) A computer-readable medium
2 embodying instructions that cause a computer to perform a method for retiring a
3 first instruction[s] processed through various processing stages, the method
4 comprising the steps of:
5 processing a second instruction different from the first instruction;
6 processing an the first instruction ~~capable of early retirement~~ until the first
7 instruction meets the criteria for early retirement;
8 indicating that the first instruction has met the early-retirement criteria;

9 processing the first instruction to a desirable stage, and at which, based on
10 an ~~the~~ indication that the first instruction has met the early-
11 retirement criteria, terminating the first instruction ~~is terminated~~ out
12 of order of a program running the first instruction; and
13 updating a state of a system processing the first instruction to reflect that
14 the first instruction has been terminated;
15 wherein the early-retirement criteria is met when processing the second
16 instruction causes ~~the instruction is processed to a point that~~
17 continued ~~execution~~ processing of the first instruction does not
18 change ~~the~~ an architectural state of the system processing the first
19 instruction, and, at the time of termination, the first instruction has
20 completed its function without completing its full pipeline.

1 11. (Currently Canceled)

1 12. (Original) The computer-readable medium of claim 10 wherein the step of indicating
2 comprises the step of generating a signal associated with the instruction.

1 13. (Currently Amended) The computer-readable medium of claim 12 wherein the method
2 further comprises the steps of:
3 sending the signal to an early-retirement unit; and
4 the early-retirement unit arranging for the first instruction to be terminated.

1 14. (Original) The computer-readable medium of claim 10 wherein the various processing
2 stages include one or more of the following stages: fetching, issuing, sorting,
3 executing, queuing, and retiring.

1 15. (Currently Amended) The computer-readable medium of claim 10 wherein ~~the~~ an
2 instruction capable of early retirement includes an identification tag for identifying
3 whether the instruction is capable of early retirement.

1 16. (Currently Canceled)

1 17. (Previously Canceled)

1 18. (Currently Canceled)

1 19. (Previously Amended Once, Currently Amended) A system for retiring a first
2 instruction[s] processed through various processing stages, comprising at least one
3 means for:

4 ~~first processing means for~~

5 processing a second instruction different from the first instruction;

6 processing ~~an~~ the first instruction ~~capable of early retirement~~ until

7 the first instruction meets the criteria for early retirement;

8 ~~second processing means for~~ processing the first instruction to a

9 desirable stage, and at which, based on an indication that the

10 first instruction has met the early-retirement criteria,

11 terminating the first instruction ~~is terminated~~ out of order of

12 a program running the first instruction; and

13 ~~updating means for~~ updating a state of the system to reflect that the

14 first instruction has been terminated;

15 wherein the criteria for early retirement is met when processing the second

16 instruction causes ~~the instruction is processed to a point that~~

17 continued processing of the first instruction does not change ~~the~~ an
18 architectural state of the system, and, at the time of termination, the
19 first instruction has completed its function without completing its
20 full pipeline.

1 20. (Currently Canceled)

1 21. (Currently Added) The method of claim 1 wherein processing the second instruction
2 comprises executing a branch condition of a branch instruction.

1 22. (Currently Added) The method of claim 21 wherein terminating the first instruction
2 includes discarding execution of a branch of the branch instruction.

1 23. (Currently Added) The method of claim 1 wherein processing the second instruction
2 comprises loading a register with a value that the register already contains.

1 24. (Currently Added) A method for retiring an instruction processed through various
2 processing stages, comprising the steps of:
3 processing the instruction until the instruction meets the criteria for early
4 retirement;
5 indicating that the instruction has met the early-retirement criteria;
6 processing the instruction to a desirable stage, and at which, based on an
7 indication that the instruction has met the early-retirement criteria,
8 terminating the instruction out of order of a program running the
9 instruction; and

10 updating a state of a system processing the instruction to reflect that the
11 instruction has been terminated;
12 wherein the early-retirement criteria is met when the instruction is
13 identified as
14 performing a logical OR of a register with the same register,
15 writing a value 0 from a register into the same register, or
16 writing a value to a register hardwired to a predetermined value.

1 25. (Currently Added) The method of claim 24 further comprises one or a combination of
2 the following steps to determine whether the early-retirement criteria is met:
3 evaluating an op-code of the instruction; and
4 evaluating a register target of the instruction.

1 26. (Currently Added) A method for retiring early a NO-OP instruction that is scheduled
2 to be processed through various processing stages, the method comprising the
3 steps of:
4 evaluating an op-code of an instruction to determine whether the
5 instruction is the NO-OP instruction, and, if so, using a tag to
6 indicate that the NO-OP instruction has met the early-retirement
7 criteria;
8 processing the NO-OP instruction to a desirable stage, and at which, based
9 on the indication that the NO-OP instruction has met the early-
10 retirement criteria, terminating the NO-OP instruction out of order
11 of a program running the NO-OP instruction; thereby skipping
12 processing the NO-OP instruction in at least one of the processing
13 stages; and

- 14 updating a state of a system processing the NO-OP instruction to reflect
15 that the NO-OP instruction has been terminated.